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Transmission Electron Microscopy to Study Gallium Nitride Transistors Grown on Sapphire and Silicon Substrates

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1. Introduction

Ever since Gallium Nitride based high electron mobility transistor (HEMT) operation was demonstrated (Khan, 1993), there is a tremendous interest in the design and growth of GaN based transistors for high power device applications. The nitride semiconductors have wide application in the fields of high electron mobility transistors (HEMTs), light emitting diodes, and various high power electronic devices. The peak electron velocity, electron mobility in GaN surpasses the best performance reported from Si based devices. GaN and related materials are highly attractive for high power and high temperature electronic devices owing to their large bandgap energy (3.4 eV), high breakdown field (3×10^6 V/cm) (Pearton, 2006) and excellent chemical stability. The growth of these nitrides layers require a substrate which should be cost effective and lattice matching to GaN. For over the past few decades, SiC, sapphire and silicon are the substrates commonly used for the growth of GaN for application as HEMTs, LEDs and other electronic devices. The choice of a suitable substrate for the growth of III-nitride semiconductor devices is very important as it influences the lattice mismatch and quality of GaN. Today most of the GaN based heterostructures (HSs) were grown either on *c*-plane (0001) sapphire or silicon. The GaN growths on silicon develop cracks due to high tensile stress and ends up in large number of threading dislocations. Poor matching between GaN and sapphire both in terms of lattice parameter and thermal expansion coefficient results in a high dislocation density as high as 10^9 – 10^{10} cm^{-2}.

The growth of low defect-density GaN is of great technological importance owing to enhanced device applications by overcoming the existing drawbacks such as current collapse and excess leakage through buffer and substrate. And for this transmission electron microscope (TEM) serves as an important tool to investigate the quality of GaN grown on various substrates. It sheds light on how the growth quality is improved by various growth advancing technologies. In this chapter, we will review how TEM continuous to play an important role in the evolution and commercialization of high quality GaN growth suitable for power device requirements.

2. Substrates for GaN

The substrates widely used for AlGaN/GaN HEMTs are SiC, sapphire and silicon. The GaN growth on SiC offers excellent quality as it has very low lattice mismatch of 3.5%. Good quality of GaN is also grown on sapphire substrate, but the thermal conductivity is very low which hinders during device operation. Therefore, Si is undoubtedly the most suitable choice for commercialization due its low cost and large size availability. Though higher lattice and thermal mismatches of Si generates a large number of dislocation and cracks, AlGaN/GaN HEMT devices on Si have shown attractive device performance for high-power applications. Until now, only Si offers a large size (8-inch diameter) wafer for growth. Table 1 compares the material properties of various substrates used for GaN growth. Therefore it is necessary to study the quality of GaN grown on Si substrate by TEM images to assess the growth quality.

Substrate material	SiC	*c*-sapphire	Si (111)
Lattice mismatch to GaN [%]	3.5	14	17.0
Thermal expansion [10^{-6} K^{-1}]	5.0	a: 7.5	2.6
(GaN : a ~ 5.5)		c: 8.5	
Thermal conductivity [W/cm • K]	4.9	0.3 ~ 0.5	1.5
Cost [per 3 inch]	US$ 2000-3000	US$ 500	US$ 100
Size available [inch]	2 to 3	2 to 4	3 to 6

Table 1. Substrates commonly used for the growth of GaN and the comparison of their properties.

Here we will be presenting how the quality of the GaN grown on sapphire and Si makes a difference in the growth quality as viewed by TEM. All the hetero-structures presented here were grown by Taiyo-Nippon Sanso, SR 4000 horizontal MOCVD set up on sapphire and Si substrates. These transistor structures grown on various substrates were reported to have excellent transistors device characteristics (Selvaraj & Egawa, 2006, 2007). In this chapter, AlGaN/GaN HEMT heterostructures grown on sapphire and Si substrates as shown in Figure. 1 will be used for TEM analysis. The MOCVD growth of GaN starts directly on sapphire substrate without any intermediate buffer layers due to reduced lattice mismatch of 14% between GaN and sapphire. On the contrary for HEMT on Si, in view of the large lattice mismatch for GaN on Si, it is necessary to reduce the dislocations by using intermediate buffer layers. The buffer layer starts with nucleation layers of 100 nm AlN followed by 40 nm AlGaN. Then, superlattice structures (multi pairs of GaN/AlN : 20/5 nm) were used as buffer of various thicknesses to reduce the dislocation density (Selvaraj et. al., 2009). The MOCVD growth completed with i-GaN channel and 25 nm i-AlGaN barrier layers as shown in Fig.1. The TEM images in the following sections will reveal how the dislocation density is lowered and the quality of the GaN was improved by increasing the thickness of the buffer.

For an excellent transistor operation and high power device application, all the layers grown and their growth quality plays a distinct role. Therefore, the growth quality of these layers will be analyzed using TEM images.

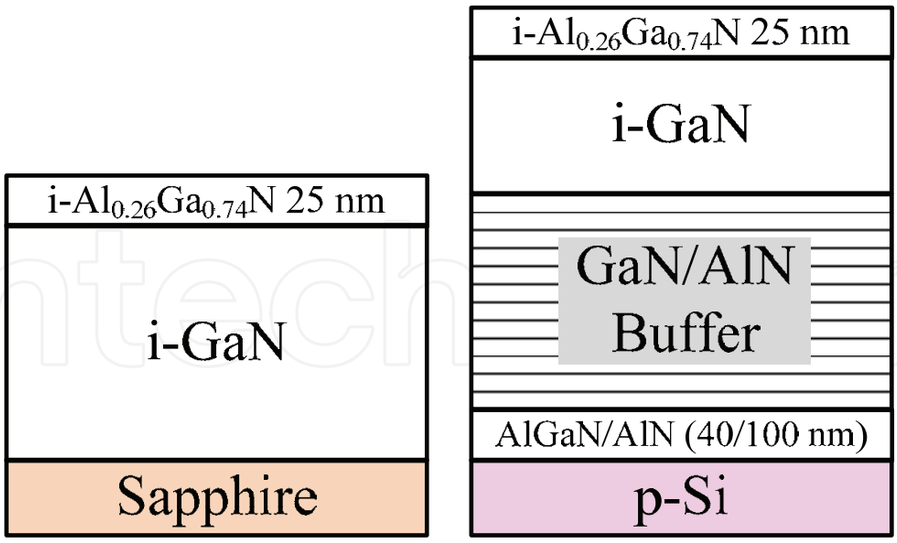

Fig. 1. The schematic description of the AlGaN/GaN heterostructures grown on Sapphire and Silicon substrates by MOCVD.

3. GaN on sapphire

Sapphire is the most extensively used substrate for growth of III-nitrides. Large area good quality crystals of sapphire are easily available at a moderate cost. They are transparent, stable at high temperature and the technology of growth of the nitrides on sapphire is quite mature. Sapphire (α-Al_2O_3) exists in four orientations namely (10-10), (0001), (2-1-10) and (11-20). The *c*-plane (0001) of sapphire has a lattice mismatch of 14% whereas the *a*-plane (11-20) has a very low lattice mismatch of 2.0% (Ambacher, 1998). The *c*-plane sapphire is widely used for GaN growth than *a*-plane sapphire. The *a*- and *c*-planes of sapphire are illustrated in Fig. 2. The growth of GaN was carried out on these two planes of sapphire namely *c*-plane and *a*-plane. With the help of TEM study, we will understand how significantly the quality of GaN changes between the these two planes of sapphire. Also the lattice mismatch of 14% and 2% respectively in the case of GaN grown on *c*-plane and *a*-plane sapphire is evident with TEM images.

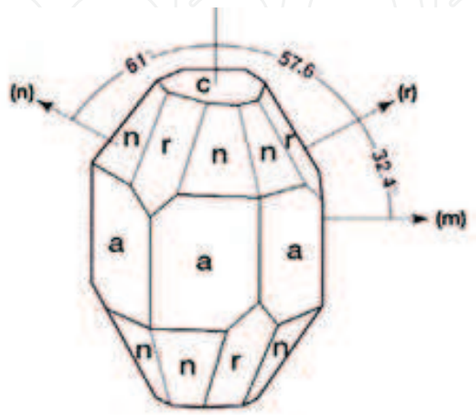

Fig. 2. Rhombohedral structure and surface planes of sapphire (Ambacher, 1998).

3.1 *c*-plane sapphire

Crystal orientations of sapphire and GaN grown on *c*-plane sapphire parallel. The *c*-plane is the commonly used orientation for the growth of GaN on sapphire. Because of the 14% lattice mismatch, a large number of dislocations are observed in the cross sectional TEM image as shown in Fig. 3. Careful observation at the interface of substrate and GaN layer shows high density of threading dislocations at the nucleation layers which begins the growth of GaN on the sapphire substrate. However, there is a decrease in the dislocation density as GaN thickness is increased. These dislocations should be minimized in view of applications for both optical and electronic devices.

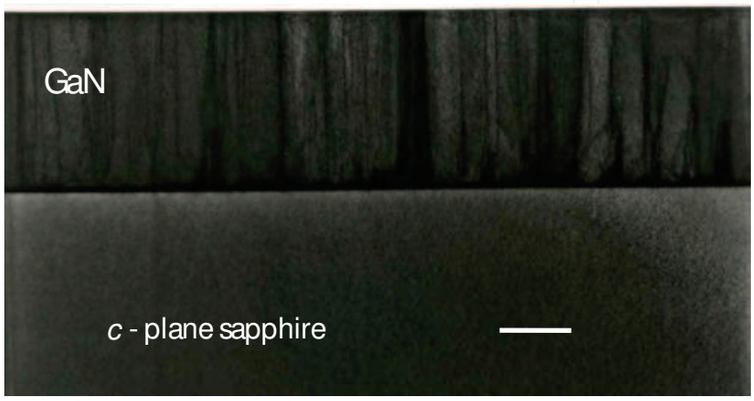

Fig. 3. MOCVD grown GaN on *c*-plane sapphire showing high density of threading dislocations (Selvaraj & Egawa, 2008).

3.2 *a*-plane sapphire

The edge and screw dislocation measured from the single crystal XRD data emphasize that dislocations are less for heterostructures grown on *a*-plane sapphire (Selvaraj & Egawa, 2008). The transmission electron microscopy (TEM) images as in Fig. 4 shows that GaN

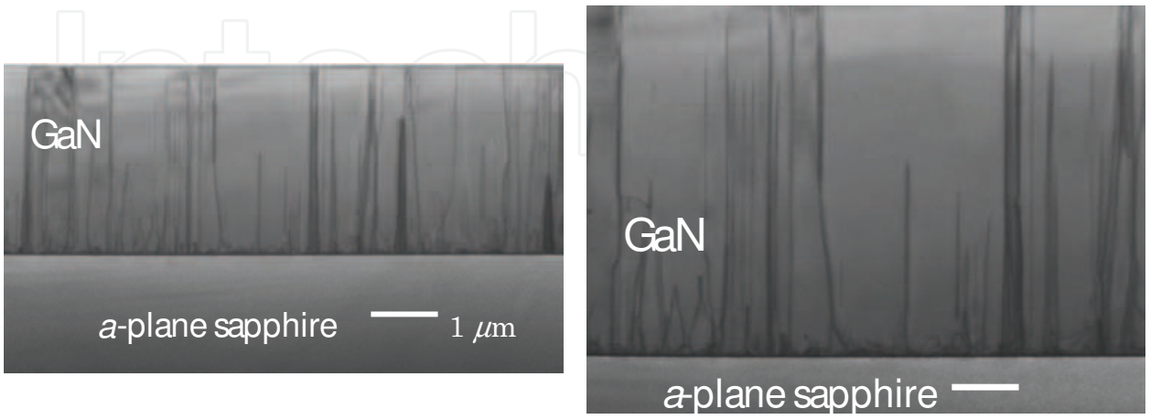

Fig. 4. MOCVD grown GaN on *a*-plane sapphire showing high quality of GaN with very low density of threading dislocations as shown in this TEM image (Selvaraj & Egawa, 2008).

grown on *a*-plane has fewer dislocations than GaN on *c*-plane as seen from Fig. 3. From the TEM images, the threading dislocation density (D_d) for GaN on *a*-plane was calculated to be lower ($1.8x10^9$ cm^{-2}) than for GaN on *c*-plane sapphire ($3.6x10^9$ cm^{-2}). These results illustrate that growth of AlGaN/GaN heterostructures on *a*-plane sapphire has good interface lattice alignment suitable for device applications.

Today *a*-plane sapphire substrate are available commercially and suitable for low cost and large scale production. The GaN grown on *a*-plane sapphire were found to have improved surface morphology with low threading dislocation density. Excellent HEMT device properties were observed with an enhanced Schottky barrier height resulting two orders of magnitude less gate leakage current and a reduced drain current collapse.

4. GaN on Si

The use of Si substrate is very promising due to low cost and large size availability. As mentioned earlier, the large lattice mismatch causes the large dislocations which affects the insulating nature of i-GaN in the heterostructure. For high power device applications, it is necessary to grow GaN on Si with low dislocations.

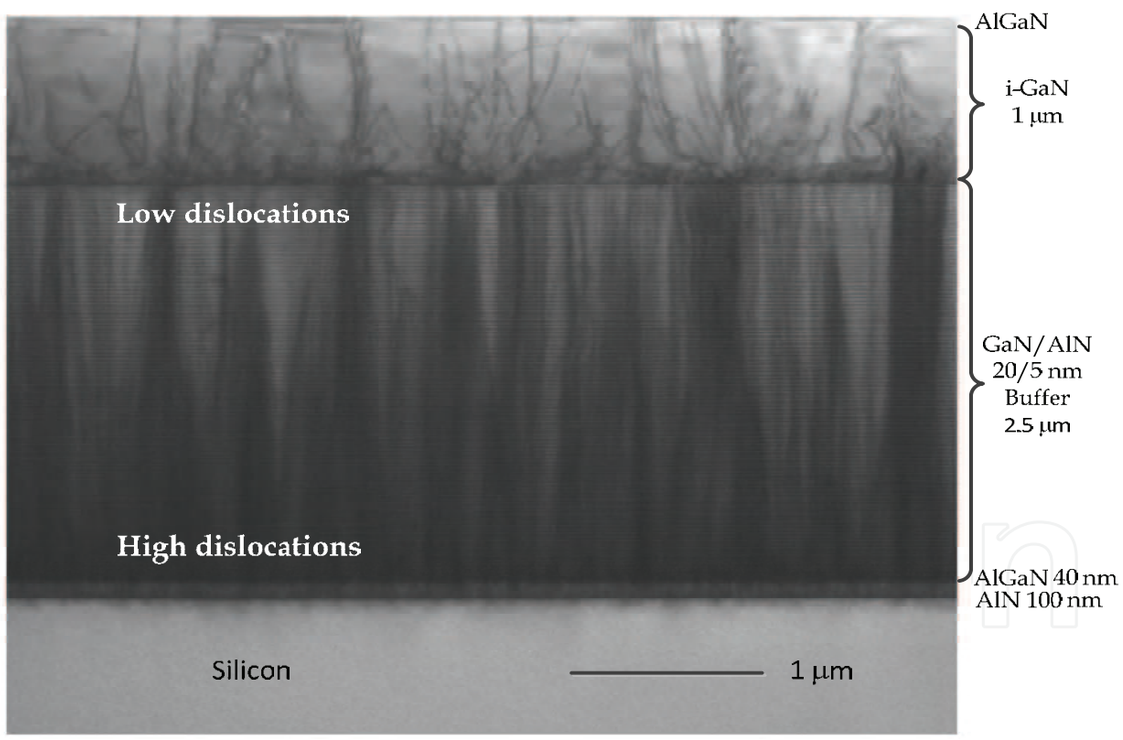

Fig. 5. TEM view of MOCVD grown GaN on silicon substrate showing improvement of GaN quality with increase in the thickness of buffer.

The GaN grown on Si with thin buffers (0.5 μm) were found to demonstrate a poor breakdown which challenges the ultimate importance of GaN for high power devices. In order to overcome the problem due to high dislocations, we have grown GaN on Si using

thick buffers which improved the breakdown (Selvaraj, 2009a, 2009b). The cross sectional TEM image for GaN grown on Si using thick buffer is shown in Fig.5 which has large threading dislocations due to 17% lattice mismatch. However the dislocations shown here are lower compared to GaN grown on Si using thin buffers. In Fig. 5, it is understood that the density of threading dislocations lowered as the thickness of epi-layers is increased. The dislocations are highest at the GaN/Si interface and gradually decreases at the top layers of the wafer. It is this top surface layer that plays a major role in the horizontal conduction of electrons through the 2DEG channel forming a high electron mobility transistor. Thus the optimization of GaN growth on Si is technologically important to achieve a commercially low cost and large area fabrication and TEM plays a major role to study the quality of epi-layers grown.

The TEM figure 5 shows the various epi-layers involved in the MOCVD growth of AlGaN/GaN HEMTs on Si. The MOCVD growth on Si starts with a 100 nm AlN layer to prevent 'Ga' melt-back etching of Si substrate at high growth temperature. The 100 nm AlN was followed by 40 nm AlGaN and both these starting layers are called nucleation layers. Then follows the buffer layer which consists of multiple pairs of GaN/AlN which is also called as super-lattice structure (SLS). The thickness of the buffer is significant to compensate the strain caused by the GaN channel layer and further lowers the dislocation density of epi-layers. In Fig. 5, the buffer consists of 100 pairs of GaN/AlN giving a buffer thickness of 2.5 μm. The multiple pairs are visible here like black and white stripe lines.

A close observation of Fig.5 shows that near the Si substrate, the density of dislocations are very high and this high dislocation density is reduced gradually as the thickness of the buffer is increased. Finally in the GaN layer which is otherwise called as channel, the dislocation density is observed to be minimum. The dislocations present in the GaN have very little effect for normal biasing conditions of the transistor. However, these dislocations are very critical for reverse blocking characteristics of the transistor. When the gate is biased below the threshold voltage during OFF-state blocking measurement, the drain is strongly biased and imperfections in the device give rise to leakage currents such as source-drain leakage, substrate leakage and gate leakage. Therefore it is necessary to minimize the dislocations for achieving a transistor capable of operating at high power conditions.

The SLS multi-pairs of GaN/AlN which forms the buffer comprised major portion among the growth completed epi-layer. The TEM image in Fig. 6 shows more enlarged view of the MOCVD grown 20 nm GaN/5 nm AlN regular periods. As the thickness of the GaN layer increase, the tensile strain in the *a*-axis of the AlN template increases (Murakawa et al., 2007). The compressive stress of the 1.0 μm thick GaN channel layer is counter balanced by the stress relief through this multiple pairs of SLS buffer. The thickness of an SLS pair namely 20 nm GaN/5 nm AlN could be confirmed through the TEM image shown here.

The use of multi-pairs of GaN/AlN facilitates lowering the dislocation density. From the TEM image shown in Fig.7 we could find that a threading dislocation running through the multi-pairs of GaN/AlN is terminated towards the top-edge of the SLS buffer. In general, the advantage of using the SLS buffer reduces the dislocation density and also provides a balance for the compressive stress produced by thick GaN channel layer.

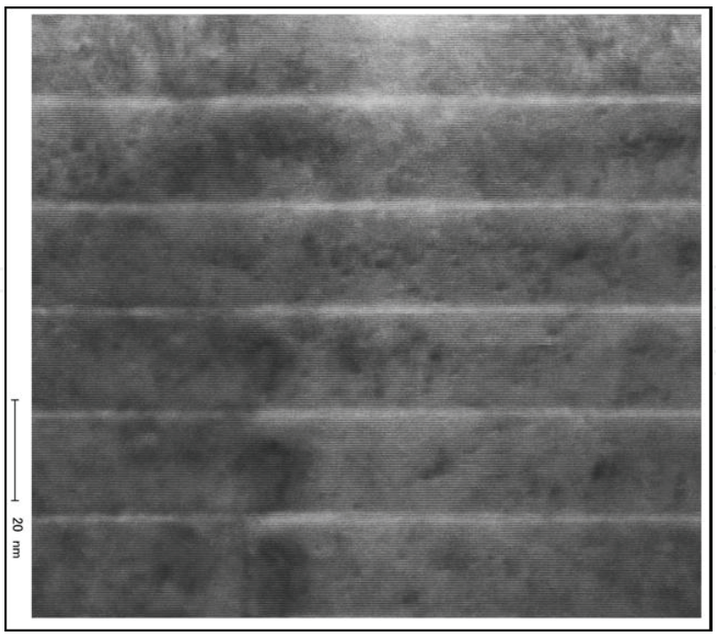

Fig. 6. The SLS buffer consisting 20 nm GaN/5 nm AlN as seen by TEM image.

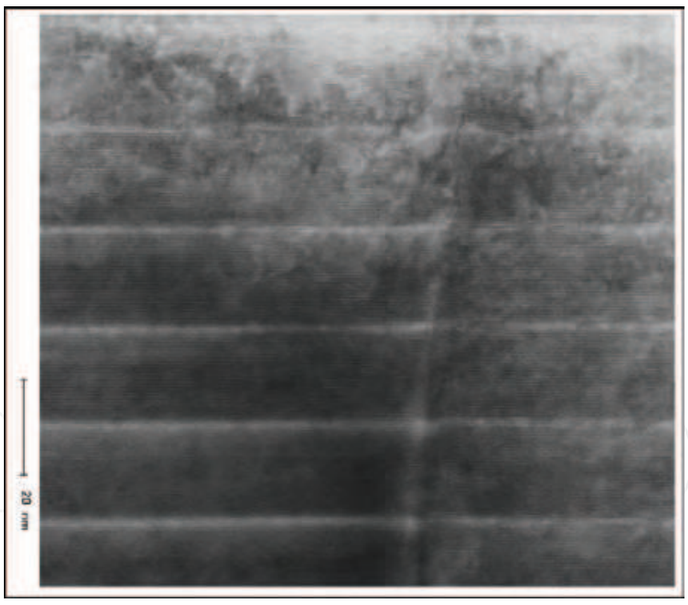

Fig. 7. Termination of a threading dislocation at the SLS buffer for AlGaN/GaN HEMTs grown on Si.

In order to find its application in the field of high power devices, we have attempted in the past to grow thick AlGaN/GaN HEMTs on Si substrate using thick GaN/AlN buffers. We found that increasing the thickness of the buffer reduces the dislocation density gradually. This was confirmed by measuring the full-width at half maximum (FWHM) from the X-ray diffraction measurement on these wafers. The screw and edge dislocation densities were

calculated from the FWHM values (Metzger et al., 1998). By growing thick buffers, we achieved lowest dislocation densities of 5.8×10^8 cm^{-2} and 2.6×10^{10} cm^{-2} respectively for screw and edge dislocation density (Rowena et al., 2011). The TEM image shown below in Fig.8 has a 2 µm i-GaN grown on 3 µm buffer. Increasing the thickness of i-GaN facilitates the growth of thick i-GaN beyond 1 µm. In comparison with Fig.5, we could observe that threading dislocations are largely reduced by increasing the thickness as shown by Fig.8. These wafers having low dislocation density showed high breakdown voltages due to low leakage currents through buffer and substrate. The buffer and substrate leakage currents which are critical for achieving a high breakdown are influenced by the dislocations and hence it is necessary to reduce the dislocations using thick buffers which compensates the lattice mismatch between Si and GaN.

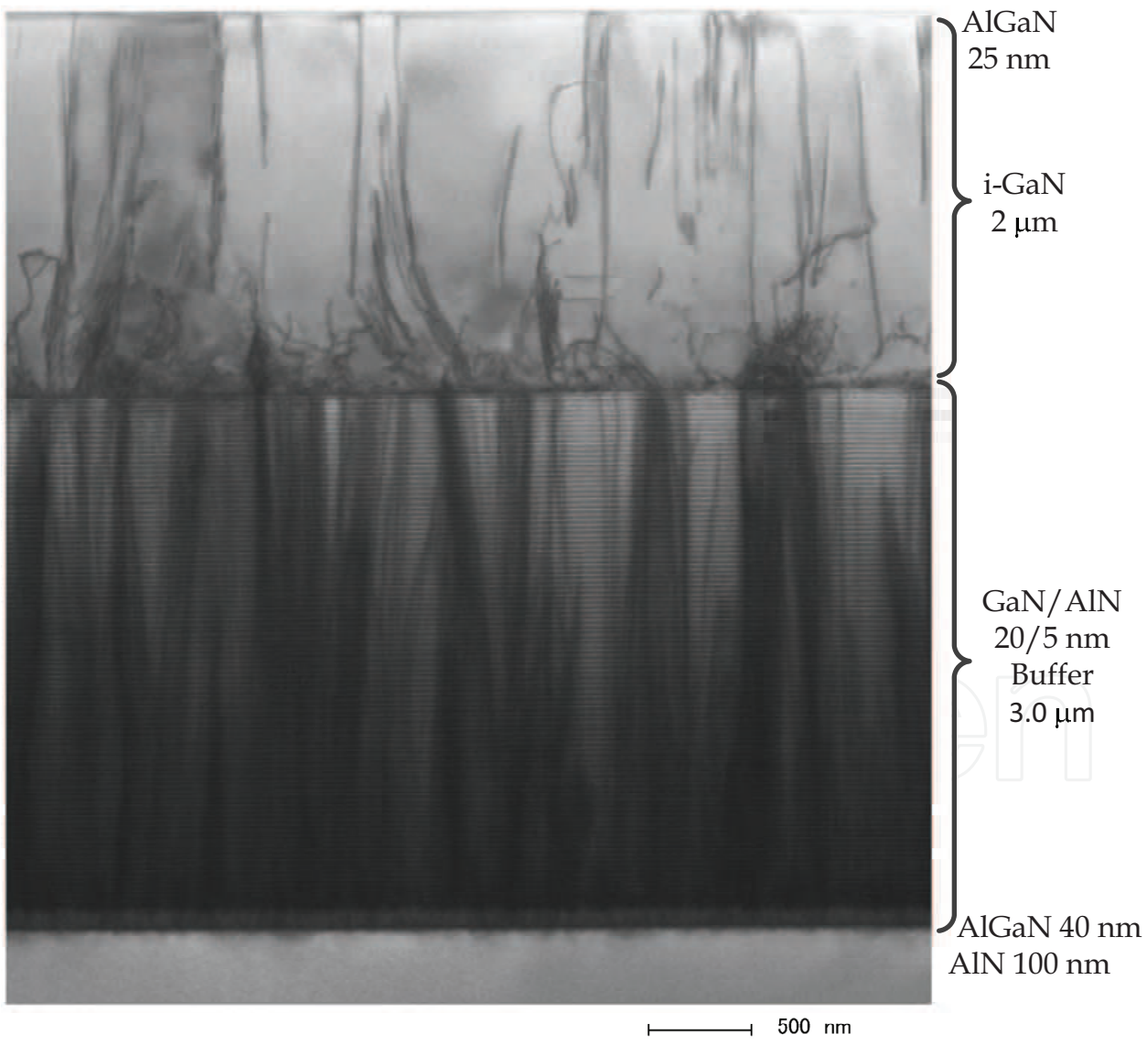

Fig. 8. A low dislocation density observed for 2 µm thick i-GaN channel layer grown on 3.0 µm thick buffer on Silicon substrate.

The 2DEG mobility of an AlGaN/GaN HEMT is around 1000 cm^2/Vs and the mobility is increased gradually all these years by improving the growth quality and other methods. One such advancement has been done by inserting a thin 1 nm AlN between the AlGaN top layer and GaN channel. This inserting 1 nm AlN layer which is called a "spacer layer", decreases the alloy disorder scattering leading to an increase in the mobility well above 1500 cm^2/Vs (Shen, 2001). A latest report demonstrate a very high mobility of 3215 cm^2/Vs which was achieved by improving the growth quality using thick buffer and using a thin AlN spacer layer at the interface of AlGaN/GaN HEMT (Selvaraj et al., 2011). The insertion of thin AlN layer produces a large discontinuity in the conduction band offset which shields the 2DEG channel from the disorder scattering. The heterostructure with 1 nm AlN layer is schematically represented in Fig.9(a). The same 1 nm AlN spacer layer is visible at the high resolution TEM image shown in Fig.9(b). Thus the highly magnified view made available using TEM helps to analyse the thin epi-layers which plays an important role in the device characteristics.

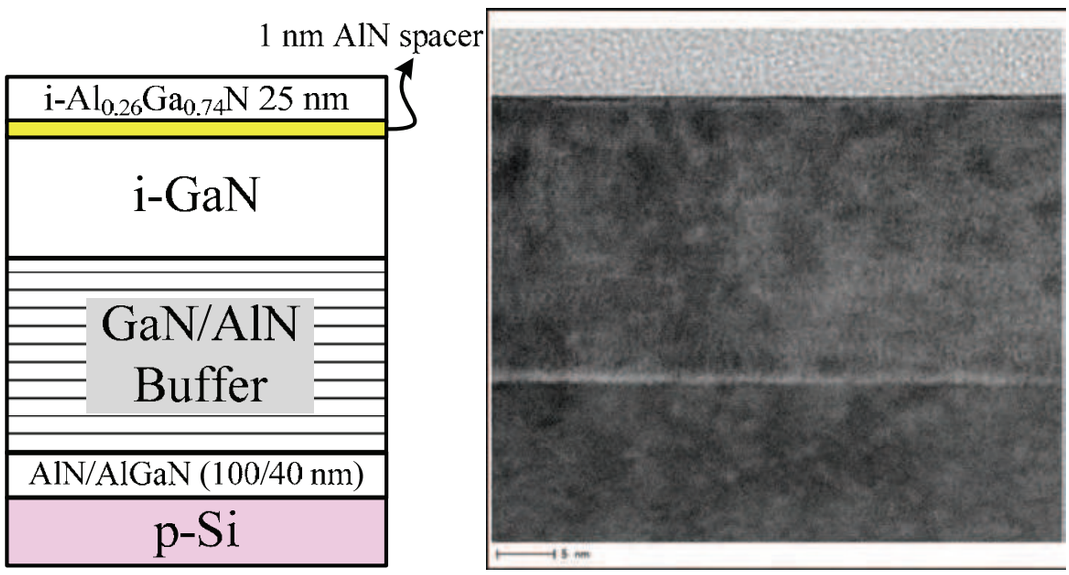

Fig. 9(a). The schematic heterostructure of an AlGaN/GaN HEMT with 1 nm AlN spacer layer; 9(b). The cross-sectional view of the 1 nm AlN spacer layer by TEM.

5. Study of defects for MOCVD grown GaN on Si

An important issue before the growth of AlGaN/GaN transistors on Si is appearance of deep-pits on surface of the growth completed wafer. These pits pose a major problem for the stability of the devices. Devices fabricated from these wafers show a high buffer and substrate leakage causing a low breakdown (Selvaraj et al., 2009). To enable the required high breakdown voltages, material quality free from bulk and surface defects is a vital concern. Deep-pits of hexagonal/polygonal shaped pyramids were observed on the on the surface of growth completed AlGaN/GaN transistors. These hexagonal pyramid shaped pits as shown by Scanning Electron Microscope (SEM) image in Fig.10 which reflects the crystal symmetry off GaN were found after growth without any intentional etching treatment. The size of these pits were around 1 to 1.5 μm in diameter.

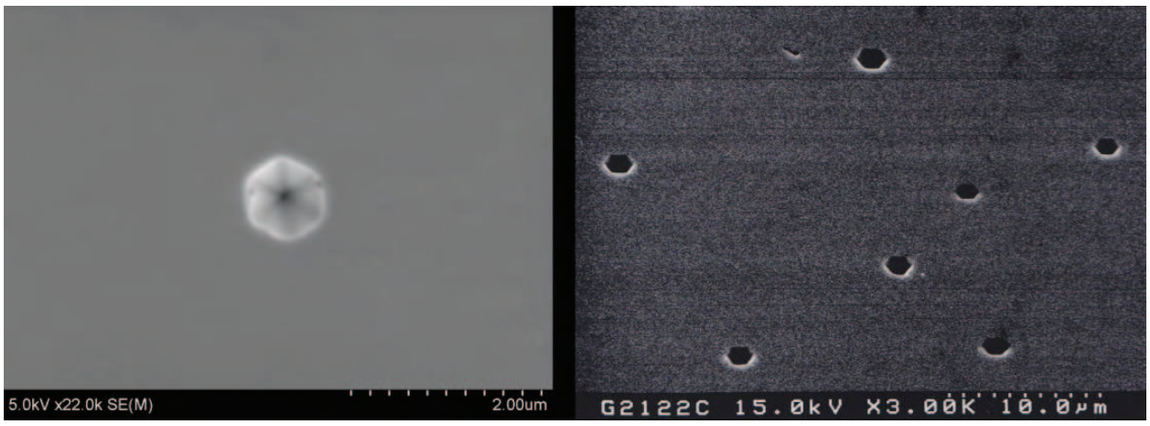

Fig. 10(a). The SEM view of the hexagonal shaped deep-pit on the MOCVD grown AlGaN/GaN layers on Si; 10(b). Another view through SEM of the deep-pits on the surface.

For AlGaN/GaN HEMTs grown on Si by MOCVD at our center, we observed density of deep-pits ranging from 900 cm^{-2} to $3x10^4$ cm^{-2}. The Fig.11 below shows the MOCVD grown AlGaN/GaN HEMTs with various density of deep-pits. It is challenging to grow a pit-free samples on Si, as the best grown wafers still have a few deep-pits. The prevention and control of deep-pits largely depend on the condition of the MOCVD growth chamber.

The HEMT devices fabricated on these wafers show an additional leakage observed through buffer and substrate finally triggering a pre-matured breakdown. When the density of deep pits are very high, there is an enormous increase in substrate leakage thereby limiting the breakdown. The three-terminal OFF breakdown voltage measured on these devices with various pit density revealed that as the pit density increased, there is a drastic reduction in the breakdown voltage. All the devices present in a single wafer with deep pits showed very poor low breakdown characteristics irrespective of the presence of deep pits at the gate-drain area. The intention of growing a thick epi-layer HEMT is to increase the breakdown so as to find its application as a high power device. But on the contrary, the presence of deep pits very much affect the device breakdown primarily due to large leakage through the buffer and substrate.

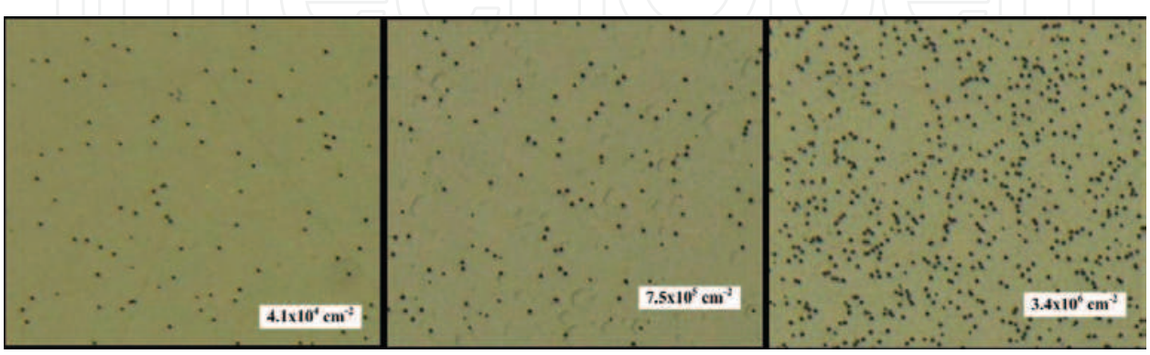

Fig. 11. Normal microscope view of the deep-pits with varying density.

The nature of these deep pits and their origin were unknown until the TEM measurement was performed on the wafers. The cross sectional images of TEM as shown in Fig. 12 revealed a hexagonal V-shaped pit originating down from the substrate and running throughout the epi-layer (Selvaraj et al., 2009). These etch pits originating at the silicon substrate run throughout the 5 μm thick epi-layer up to the AlGaN surface causing deep surface pits. And even using a thick buffer layer could not stop the deep pits reaching the AlGaN surface layer. These deep pits found on surface originate from the substrate and behave like micro-pipes for high substrate leakage flow which in turn affects the breakdown of the devices.

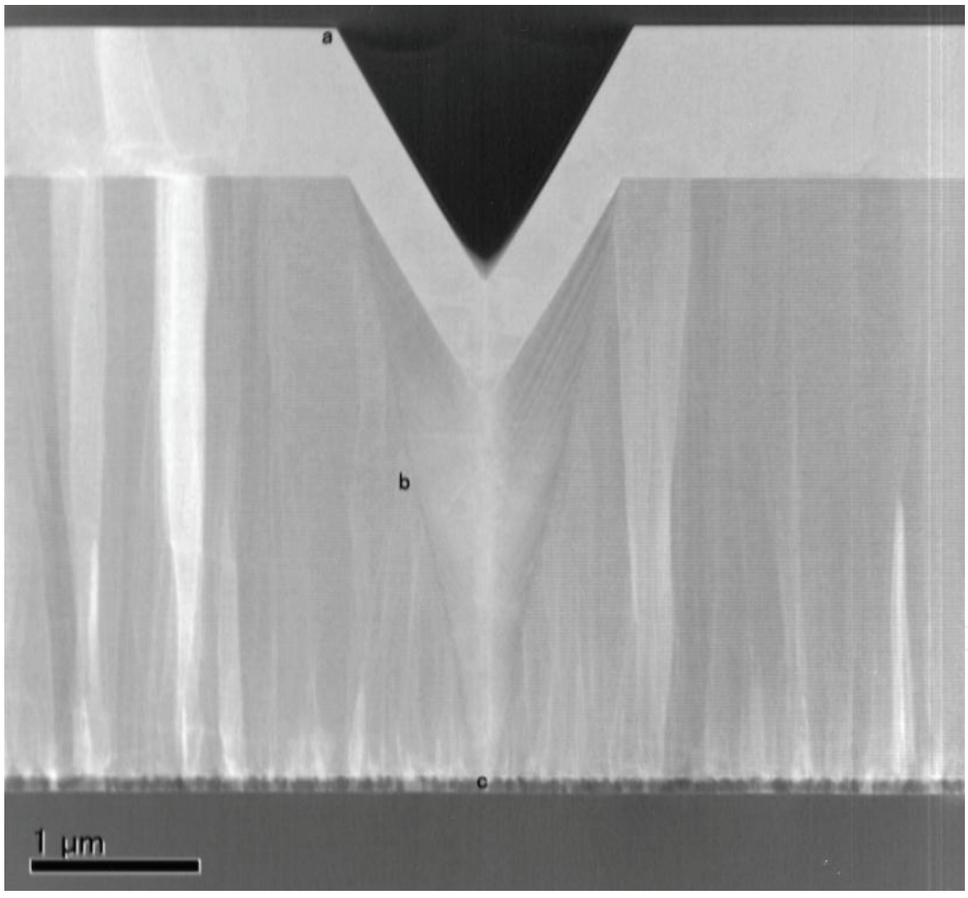

Fig. 12. MOCVD grown GaN on Si having a deep-pit on the surface. The TEM image reveals the origin of pit from the Si substrate causing high substrate leakage current.

Recently we also made an in-depth study on the regions around deep-pits and their limitations on the performance of MOCVD grown AlGaN/GaN HEMTs on Si substrate (Selvaraj et al., 2011). We found that for regions within 50 µm distance of deep-pits, there is a degradation observed in device performance. If the active region of the HEMTs are within the 50 µm distance from a deep-pit, then it leads to 19% decrease in the drain current and positive shift in the device threshold voltage signifying an early pinch-off. The early pinch-off for devices within the 50 µm distance of deep-pit confirms the presence of high dislocations causing dislocation scattering. These high dislocations cause 50% decrease in 3-terminal OFF breakdown voltage due to large buffer and substrate leakage current. Further, the 50 µm radius defective region around the pits were confirmed by cathodoluminescence and Raman shift measurements. Therefore, for AlGaN/GaN epi-layers grown on Si having a low density of deep-pits on the surface, the pits does not impede the normal performance of the HEMTs if the source/drain active region is located far away from the deep-pits. As the appearance deep-pits were due to melt-back etching of Si substrate by 'Ga' at high growth temperature, it is imperative that GaN growth on Si substrate is free from deep-pits for cost-cutting measures.

6. Conclusions

The TEM plays an important role in identifying the quality of GaN grown on various substrates. Further it helps in understanding the cause for failure modes arising in the devices. TEM assists in designing GaN based devices for high power device applications. In this chapter, it was discussed regarding the application of TEM for investigating the growth of Gallium Nitride on various substrates. Sapphire substrates in different planes (*c*-plane & *a*-plane) and Silicon were used for the growth of AlGaN/GaN high electron mobility transistors. The GaN grown on *a*-plane sapphire offers the best quality. Because of the use of thick buffer layers, good quality GaN were observed on Si substrate inspite of large lattice mismatch. The MOCVD grown AlGaN/GaN layers on Si had varying density of deep-pits and subsequently the devices fabricated from those wafers showed a large leakage through buffer and substrate. The reason for the leakage was understood by taking TEM images across a deep-pit. These deep-pits had an origin from the Si substrate, probably due to melt-back etching of Silicon by 'Ga'. It was with the help of TEM we found that these deep-pits are the defects behind the high leakage currents observed in the wafers. Thus, the TEM measurement provides a very important technological support for analyzing the growth of device quality epi-layers.

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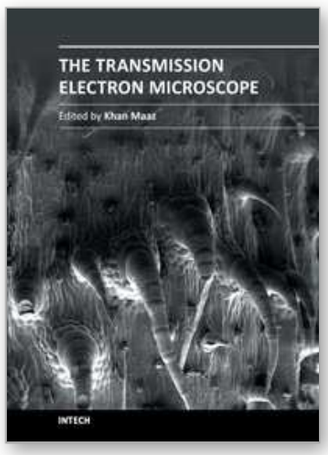

The Transmission Electron Microscope

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The book "The Transmission Electron Microscope" contains a collection of research articles submitted by engineers and scientists to present an overview of different aspects of TEM from the basic mechanisms and diagnosis to the latest advancements in the field. The book presents descriptions of electron microscopy, models for improved sample sizing and handling, new methods of image projection, and experimental methodologies for nanomaterials studies. The selection of chapters focuses on transmission electron microscopy used in material characterization, with special emphasis on both the theoretical and experimental aspect of modern electron microscopy techniques. I believe that a broad range of readers, such as students, scientists and engineers will benefit from this book.

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